

# PCB Layout Guidance

©ACEINNA, Inc.

One Technology Drive, Suite 325, Andover, MA, 01810, USA

Tel: +1-978-738-0900, Fax: +1-978-738-0196, [www.ACEINNA.com](http://www.ACEINNA.com)

Information furnished by ACEINNA is believed to be accurate and reliable. However, no responsibility is assumed by ACEINNA for its use, or for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of ACEINNA. ACEINNA reserves the right to change this document without notification.

## 1. Thermal Rise

Resistance heating effect due to current flow through primary current path should be considered during the design of any current sensing system. The resistance of the isolated primary current path through the Current Sensor IC, PCB trace resistance and contacts to the PCB will generate thermal heat as current flows through the system.

The thermal rise is dependent on PCB layout, trace width, copper thickness, cooling techniques such as copper flood with vias, and the profile of the primary current.

Although the primary resistance is extremely low, it still can cause a fair amount of on-chip power dissipation when the current is high. If the heat is not dissipated properly on the PC board, the temperature of the junction may reach the threshold and the surface would be hot. A good PCB Layout can mitigate the thermal stress and therefore eliminate this issue.

- Use large PCB copper areas for high current path, including IP+ and IP-. It helps to minimize the PCB conduction loss and thermal stress.
- Increase the thickness of the copper layers for high current, which reduces conduction loss as well.
- Add thermal vias surrounding the solder pads of IP+ and IP-.

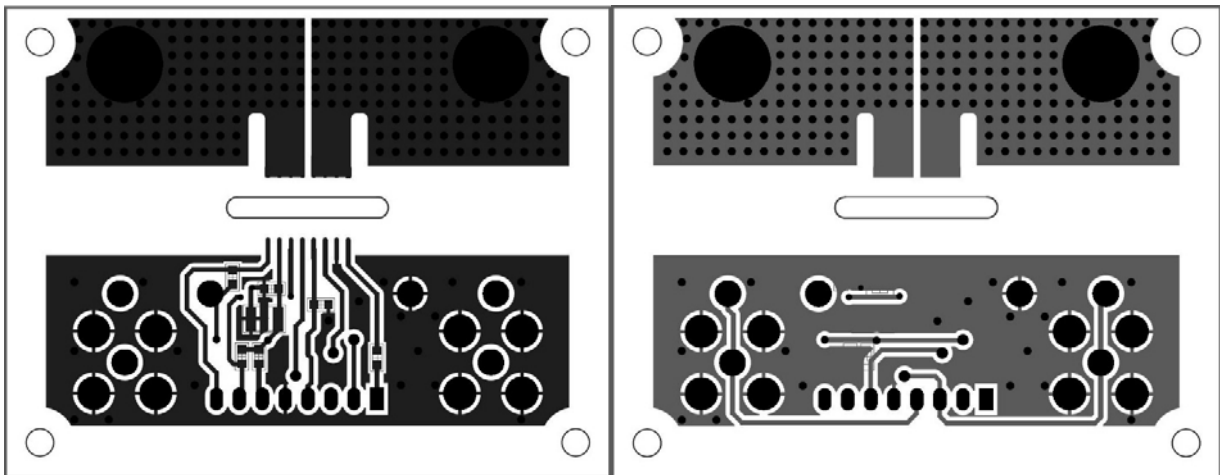


Figure 1: Top and Bottom Layers for MCx1101 Evaluation Board

## 2. Primary Current Flow Direction

Current is sensed by measuring the magnetic field generated by the current flowing through the internal current path. The direction and proximity of all current-carrying paths have impact on the sensor IC's performance. For optimal performance, it is highly recommended that the primary current should approach the IC parallel to the current-carrying pins, and avoid current-carrying trace creeping towards the center of the package to avoid and or minimize magnetic fields due to external PCB traces. Refer to Figure 2.

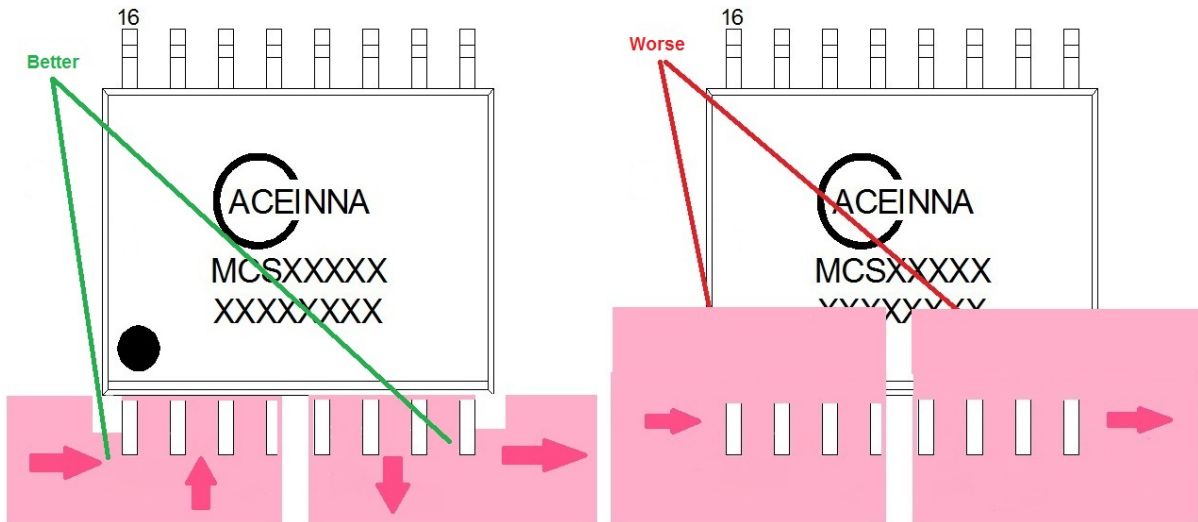


Figure 2: To guarantee the direction of the primary current paralleling to the current-carrying pins.

### 3. Isolation

The slot under the IC on the PCB, as shown in Figure 3, is a good practice to help improve for isolations.

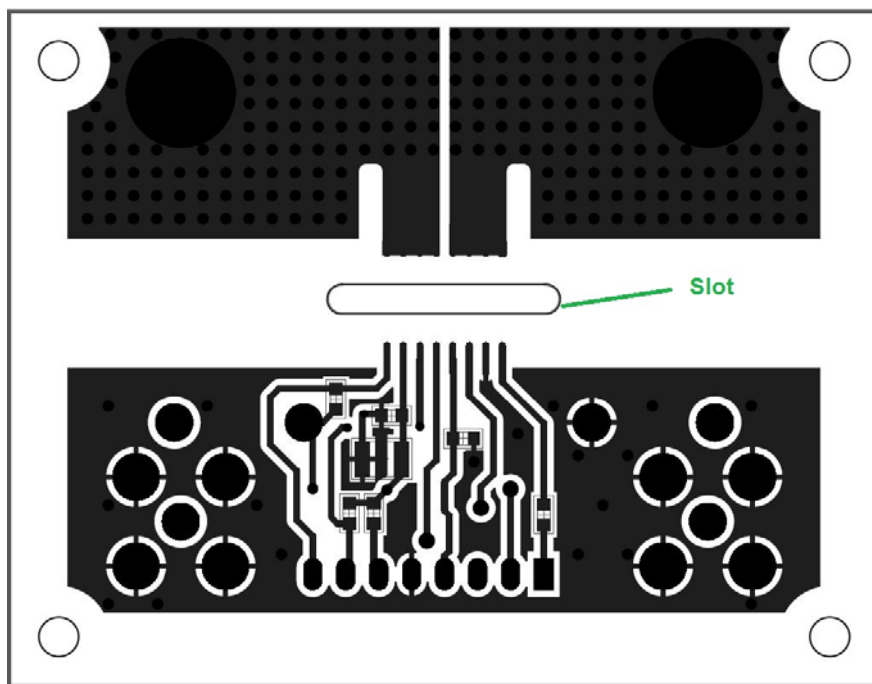


Figure 3: Slot under IC on the PCB

### 4. Components location

- Place bypass capacitor C2 as close as possible to the IC, between the VCC and the GND pins to help improve noise performance substantially. A 0.1uF ceramic capacitor is recommended.
- Place bypass capacitor C1 as close as possible to the IC, between the VREF and the GND pins to help improve noise performance substantially. A 10nF ceramic capacitor is recommended
- Connect pin15 “GND” to signal GND.