Design Considerations of Digital Controlled Totem Pole PFC

Higher efficiency and size are always an important concern in the design of a switching mode power supply, especially for energy saving and environmental protection

Worldwide, the Electronics Industry is seeing substantial changes – driven by Artificial Intelligence, cloud based IoT, next generation RF technologies, Electric Vehicles (EV) and their Advance Driver-Assistance Systems (ADAS) and Autonomous Driving needs, – to the widespread adoption of wide-bandgap power switches based on Silicon Carbide (SiC) and/or Gallium Nitride (GaN) semiconductors. The overall global electrical power demand is also rapidly increasing and is also driving additional demand.

These trends put lots of pressure on power engineers and architects to extend existing power technology boundaries to achieve higher system efficiencies, faster response times, and reliable and robust, smaller size solutions with reduced part counts for lower cost in new generations of electronics system designs.

One such example is power supplies that are pushing to meet 80 Plus Titanium efficiency levels for wide variety of power conversion applications such as telecom, server and data center or other industrial power supplies. To meet the power efficiency and size improvement goals, design of systems need to exploit the advancement in power switches and utilize better suited architectures and solutions in the circuit. The fast switching wideband gap Silicon Carbide (SiC) or Gallium Nitride (GaN) power switches and isolated single chip current sensors in bridgeless Power Factor Correction (PFC) and DCDC converters helps to improves efficiency and thermal management, and to reduce both size and component count to simplify PCB circuits.

Introduction

Higher efficiency and size are always an important concern in the design of a switching mode power supply, especially for energy saving and environmental protection. The Energy-Star 80 PLUS efficiency specification (introduced in 2007) adds higher efficiency levels for AC/DC rectifiers from Gold to Platinum and on to the Titanium level.

80 plus test type	115V internal Non-redundant				230V internal Redundant			
Fraction of rated load	10%	20%	50%	100%	10%	20%	50%	100%
80 Plus		80%	80%	80%				
80 Plus Bronze		82%	85%	82%		81%	85%	81%
80 Plus Silver		85%	88%	85%		85%	89%	85%
80 Plus Gold		87%	90%	87%		88%	92%	88%
80 Plus Platinum		90%	92%	89%		90%	94%	91%
80 Plus Titanium		92%	94%	90%		94%	96%	91%

Table 1: 80plus Efficiency Standard@1

To meet the 80 Plus Titanium standard, the power supply design needs to achieve 96% Titanium peak efficiency. This means that the target efficiency of Power Factor Correction (PFC) circuit efficiency should be 98.5% for both 115V and 230V input condition overall efficiency of 96% if DCDC Converter efficiency is assumed to be 97.5% (98.5%*97.5%=96 %). In order to achieve that high efficiency level, the most suitable topologies are bridgeless PFC circuits, which do not require a full-wave AC rectifier bridge, and hence reduce related conduction losses. There are two types of bridgeless PFC designs: Bridgeless PFC and Totem Pole PFC (Figures 1A and 1B)

In this paper, we will focus on the design of a 3.3kW Totem Pole PFC. Compared to bridgeless PFC, Totem Pole PFC removes the input bridge rectifier and also uses a MOSFET (Metal Oxide Semiconductor Field Effect Transistor) to replace the rectify diode to greater improve overall efficiency further.

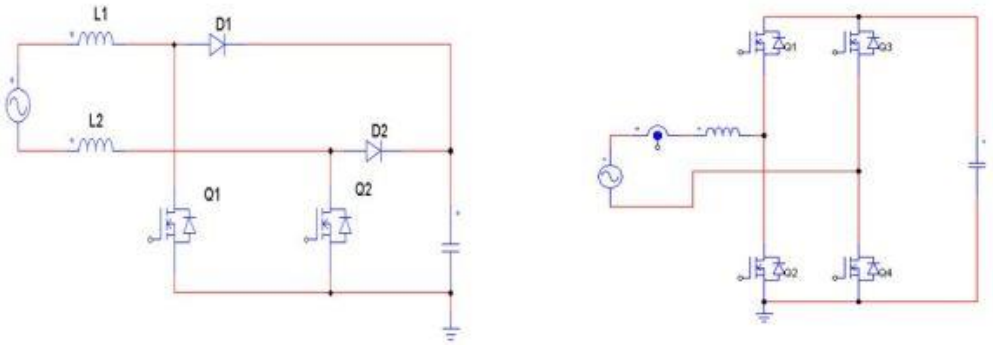

Figure 1: a) Bridgeless PFC, b) Totem Pole PF

Design Consideration of Totem Pole PFC

Why SiC-MOSFET is needed in Totem Pole PFC design

As Figure 2 shows, Totem Pole PFC can be considered a synchronous-rectified boost DCDC converter. (A DCDC boost converter provides output voltage higher than the input voltage.) For a synchronous-rectified boost, a big problem is reverse recovery charge of the MOSFET body-Diode if the converter works in CCM (Continuous Conduction Mode) condition. This means that the Totem Pole PFC can only work in DCM (Discontinuous Conduction Mode) or BCM (Boundary Conduction Mode) mode with traditional Si-MOSFET. But both have challenges.

A DCM PFC can only support low power applications. When using a BCM PFC, the operation frequency varies widely. In addition, the peak current will be 2 times of a CCM PFC, which increases the difficulty of EMI filter design and efficiency optimization. With the availability of fast switching wideband gap transistor SiC and GaN based power switches, which have minimal reverse recovery charge along with other advantages, Totem Pole PFC designs can now operate in CCM mode to provide higher efficiency and higher power.

In the paper, we will discuss a Totem pole architecture and design based on SiC MOSFETs, magnetic current sensing and CCM control. We chose a SiC-MOSFET C3M0065090K from Wolfspeed as the high frequency switches and a IXFH80N65X2 from IXYS as the low frequency switches. The choice of SiC-MOSFET over GaN-MOSFET is based on SiC-MOSFET providing higher breakdown voltage needed for this application. Using a SiC-MOSFET can dramatically reduce the reverse recovery loss enabling the Totem Pole PFC to work in CCM mode to support higher power. Si-MOSFET to SiC-MOSFET provide different amounts of body-Diode loss.

Table 2 compares the amounts of reverse recovery loss between Si-MOSFET and SiC-MOSFET. It is clear that SiC device dramatically reduces the body-Diode loss. The chart demonstrates that the reverse recovery loss of SiC-MOSFET is only $1/6^{th}$ of Si-MOSFET.

	Si Mosfet	C3M0065090K
Vds	400	400
Id	12.4	20
Qrr(uC)	0.77	0.13
fs(KHz)	60	60
Loss(W)	18.48	3.12

Table 2: Body-Diode loss comparisons@2

Positive Half Line Cycle Operation

The positive half line cycle operation of the totem-pole PFC is shown in Figure 2.

Q1 and Q2 are fast switching SiC-MOSFET devices (operating at high carrier frequency) Q3 and Q4 are traditional lower speed Si-MOSFET devices (operating at 50 or 60Hz) There are only two semiconductor devices in the current path in totem-pole PFC. In positive half line cycle, Q1 acts as main switch and Q2 acts as a synchronous-rectifier MOSFET, Q3 is always on and acts as a resistor. When Q1 is on, the ac source stores energy in the inductor and the output capacitor supports the load current. When Q1 is off and Q2 is on, the ac source and energy in inductor support the output current and charge the output capacitor.

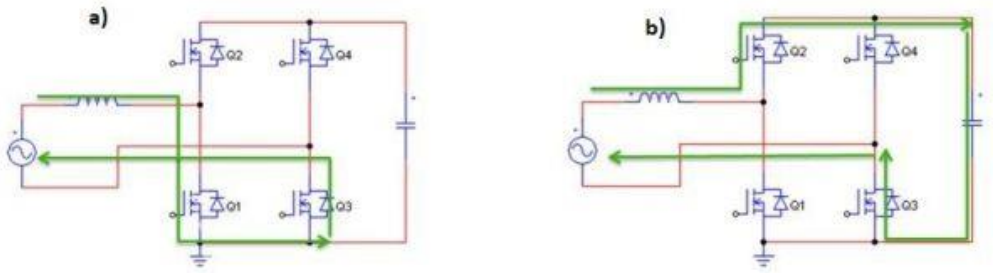

Figure 2: a) Q1 and Q3 on, b) Q2 and Q3 on

Negative Half Line Cycle Operation:

The negative half line cycle operation of the totem-pole PFC is shown in Figure 3.

Again, there are only two semiconductor devices in the current path. In the negative half line cycle, Q2 acts as main switch and Q1 acts as a synchronous-rectifier MOSFET. Q4 is always on and acts as a resistor. When Q2 is on, the ac source stores energy in inductor and the output capacitor supports the load current. When Q2 is off and Q1 is on, the ac source and energy in the inductor supports the output current and charge the output capacitor.

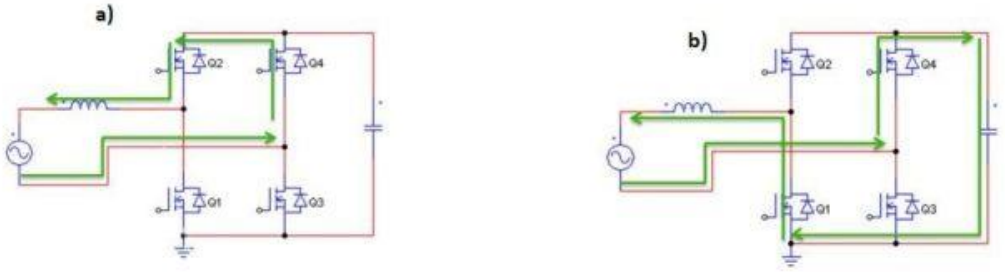

Figure 3: a) Q2 an Q4 on, b) Q1 and Q4 on

Current Sensing

In PFC applications, average current mode control is used mostly because it is simple and accurate. For average current mode control, average inductor current is required for the current control loop.

For traditional PFC designs, typically a shunt is placed in the ground line to sense current as shown in figure 4a. A shunt resistor is used to sense the input current and an amplifier is used to get different gain. The method is the simplest way to sample the input current. In contrast, using Totem Pole PFC design, there is no ground line and the circuit can't sample the current similarly as in traditional PFC.

For Totem Pole PFC, there are several methods to sample the inductor current: 1) Current Transformer (CT) as shown in figure 4b, 2) Shunt resistor with an Op-amp and an isolator as shown in figure 4c, 3) Magnetic Current Sensor Modules or ICs as shown in figure 4d.

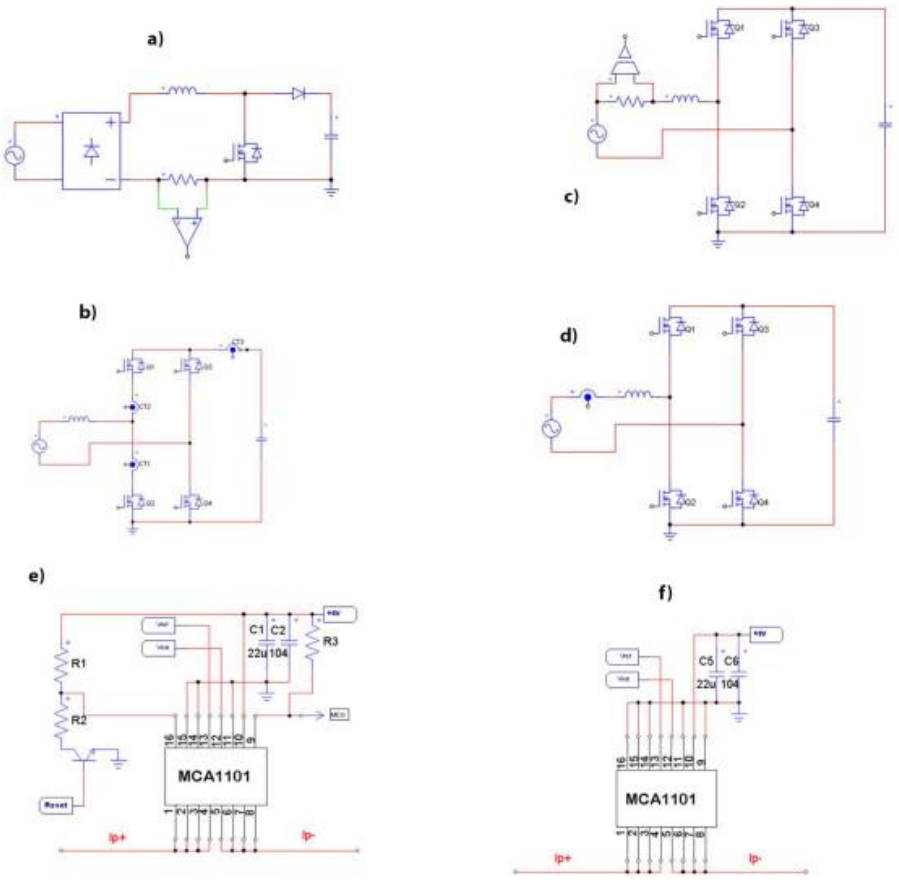

Figure 4: a) Traditional PFC current sensor, b) Current Transformer (CT), c) Shunt resistor with Opamp and isolator, d) Magnetic current sensor module or IC based on Hall Effect or AMR sensor, e) MCA1101 application circuit with OCP function, f) MCA1101 application circuit without OCP function

Current Transformer

A current transformer (CT) can be used to sample the inductor current. However, as a current transformer can only work in AC, they are better for high frequency designs. To sense switching current, three CTs are needed to sample and integrate the inductor currents in positive and negative cycle through MOSFET and rectifier. Figure 4b shows the typical position CT. CTs provide the measurement isolation. Although separate isolated power is not needed for CTs, the circuit requires three CTs to reconstruct the line current. Unfortunately, CTs also suffer from linearity and hysteresis impact over temperature. Other challenges are that using three CTs increases costs and takes up more space.

Shunt with op-amp and an isolator

Another method is to insert a current shunt in series with inductor as shown in figure 4c. This approach requires an op-amp, an isolator, and a separate isolated power supply with multiple passive components around the isolator and op-amp. The circuit design is complex and needs more space. Additionally, for higher current applications, using accurate low value resistors to minimize power dissipations are also costly. Further, output response time is limited due to opto-isolator and op-amp on signal path. The combined output step response time can easily be over 1us.

Non isolated current measurement using shunt with an op-amp (without an isolator), typically used in the ground return of traditional PFC, shown in Figure 4a, is not suitable for Totem Pole PFC, which requires isolated current measurements.

Magnetic Current Sensor Module or IC

An isolated magnetic current sensor module or IC with Hall Effect or AMR magnetic field sensors is an effective and popular method of current sensing. These magnetic current sensors provide the required isolation and do not need separate isolated power supplies. The typical sensor location is showed on figure 4d.

However, there are 2 major challenges to overcome on the selection of magnetic current sensor

1. Limited Bandwidth of magnetic current sensors: The traditional Hall Effect based sensor module or ICs with typically 120kHz bandwidth, has 3db distortion in 120kHz. Although it can be used for 50Hz PFC current, its slow output response time (related to bandwidth) can't support the fast response time needed for peak and over current protection. For fast switching current it'll cause delay for peak current protection. Also, in practical applications, current measurement is typically done at the middle of the switching PWM pulses. For this, current sensor IC or module needs to support the higher bandwidth needed for measuring current at high switching frequency in SiC or GaN based Totem Pole PFC.

- The big size of the current sensor modules: The current sensor modules typically that utilize ferrite core with Hall Effect sensor. The choice of such a magnetic

current sensor module needs to be accurate with high bandwidth with low phase delay and fast output response time for measurement and protection. The size of current sensor modules impacts the space needed and therefore power density of the PFC solution. Additionally, high bandwidth and accurate current sensor modules are costlier.

In this design, a high accuracy 4.8kV isolated current sensor IC (MCA1101-50-5) from ACEINNA was chosen to sample the inductor current. This +/-50A current sensor IC with 0.6% typical accuracy, 1.5 MHz bandwidth, and output response time of 300ns can fully meet the high frequency current sample measurement and protection requirements in this design@3. It provides reinforced isolation and meets UL60950 with no additional isolated power supply. Typical application circuit is shown in Figure 4e. If internal Over Current Detection (OCD) function is not used, only decoupling capacitors are needed further simplifying the circuit as shown in Figure 4f.

MCA1101 current sensor IC provides accurate 0A reference voltage output pin which helps to calibrate out 0A offset in the system. The Over Current Detection (OCD) threshold can be set on the IC and fault flag pinout can interface with MCU, to trigger the over current protection in the software. This single chip current sensor solution, is in a space saving small IC package, shown in Figure 5a and 5b, compared to bulky modules.

The MCA1101 provides many advantages for Totem Pole PFC application. These include high accuracy over temperature, high bandwidth, fast response, single power supply, reinforced isolation, programmable over current detection (OCD) voltage and fault pin to provide current information to MCU. All of these merits make the AMR based current sensor chip to be an attractive solution for the inductor current sample in this Totem Pole PFC design.

Figure 5: a) MCA1101 current sensor IC, b) Inside of MCA1101

Power Design

Power Switches (SiC-MOSFET and Si-MOSFET) Selection

From the analysis, one leg (Q1, Q2) works in high frequency and another leg (Q3, Q4) works in line frequency. To choose a suitable MOSFETs, we need to calculate the voltage, current and power loss in the MOSFETs.

For the high frequency leg, we know that during the positive cycle, Q1 acts as a main switch and during negative cycle, Q1acts as a synchronous-MOSFET.

The RMS current flow through Q1 can be calculated as below. For switching loss, it also can be calculated as below

$$Psw := \frac{\sum_{k=0}^{1200} \left[\frac{\left| Ia\left(\frac{k}{fs}\right) \right| \cdot Vo \cdot (toff + ton1)}{2} \right]}{1200} \cdot fs$$

From the equations above, to minimize switching power loss, we choose Wolfspeed 4Pin SiC-MOSFET C3M0065090K, 900V, 65mohm devices for the high frequency switches Q1 and Q2 for this application. The device has a fast intrinsic diode with low reverse recovery (Orr) and has very low output capacitance (60pF).

For the low frequency Si-MOSFET (Q3 and Q4), the RMS Current flow through can be calculated as below. The Power loss is mainly due to Rds(on). So, we selected the low Rdson MOSFET IXFH80N65X2 because of its high level of efficiency.

$$Ilf := \sqrt{Fline \cdot \int_0^{\frac{1}{2 \cdot Fline}} (Iinrms \cdot \sqrt{2} \cdot \sin(2 \cdot \pi \cdot Fline \cdot t))^2 \, dt}$$

Inductor Design

The input inductor is designed to keep the current ripple under 30% of the maximum peak input current, I_{pk_pk}. The maximum peak input current occurs at low line and at full load. The equation below gives the minimum inductance to operate in CCM at full load. D is the duty ratio of the active switch (Q1 or Q2) of the fast switching leg.

Inductance Solution	
F	65Khz
Irms	20 A
Ipeak	28 A
L @ 0 A	622.728μH ±10%
L @ 20 A	235.26μH (H=158.36Oe)
L @ 28 A	148.8μH (H=221.70Oe)
Core Loss	3.391238 W
Copper Loss	11.792W
Total Loss	15.18278 W

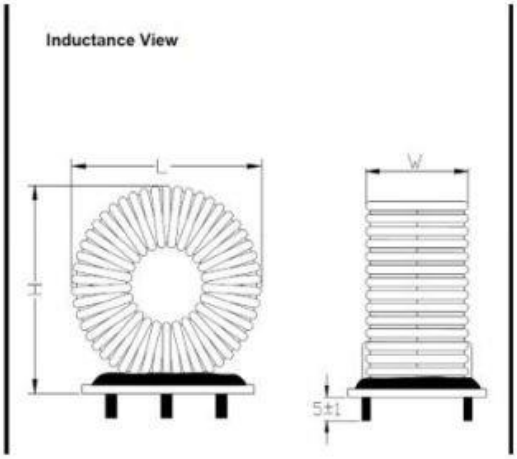

Table 3: PI191139V1 Inductor data

V out is the 400 V DC output voltage and the fsw is the switching frequency. For this design, the minimum inductance value is therefore 200μH. When calculating the formula, we choose PI191139V1 as Table3

$$L \geq \frac{D(1-D)}{\Delta I_{pk_{pk}} f_{sw}} . Vout$$

Output Capacitor

The output capacitance is determined based on two constraints: load hold-up time and output voltage ripple regulation. In this design, the hold-up time is set to be 10ms and the output voltage peak to peak ripple is set to be 30 V.

$$C_{out} \geq \frac{2P_0 t_{holdup}}{{V_0}^2 - {V_{0\_min}}^2} \; ; \; C_{out} \geq \frac{P_0}{2V_0 \pi f_{line} V_{ripple}}$$

So, we choose 2pcs of HP 450V560μF (30×50) capacitor are used in parallel to meet the requirements.

Totem Pole PFC Control Block Diagrams and Circuit Simulation

The Totem Pole PFC control block diagram is shown in Figure 6 and related application control circuit is shown in Figure 7. The simulation results in Figure 8 shows that the PFC circuit can work well.

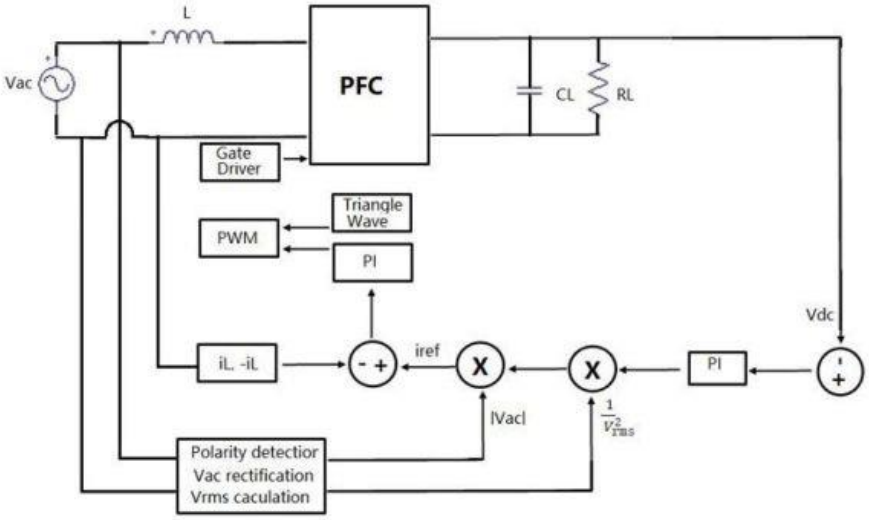

Figure 6: Totem Pole PFC control block diagram

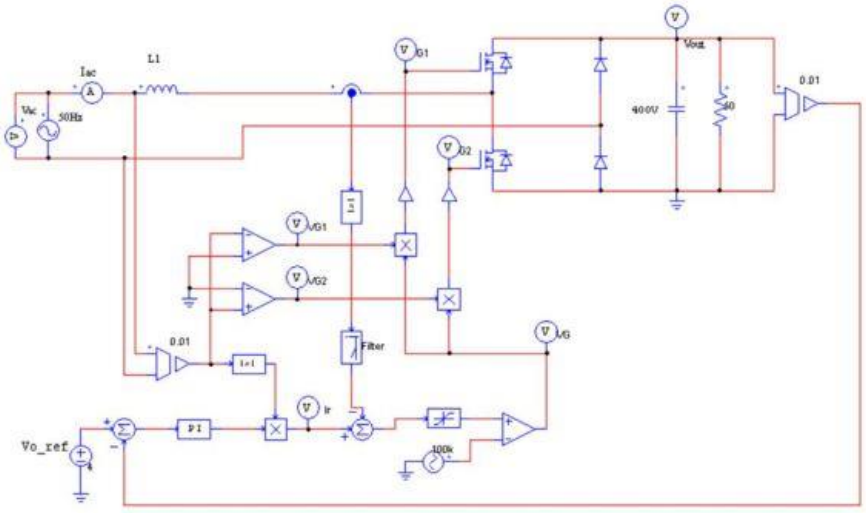

Figure 7: The application control circuit

1. Reference current Iref = K(Vdc-Vdc_ref)*|Vac|*1/V ²rms

K is depends on Proportional-Integral time constant
(**Vdc-Vdc_ref**) is the output voltage error
|Vac| is the follower factor between the voltage and current
1/V ²rms is the power limitation factor

- Input loop current **IL** must be monitored cycle by cycle accurately and needs control loop pole placement for stability.
- The current error **Δi** = (k1*IL+k2*∫IL)-Iref, it is key parameter for the average current mode control. K1 is linear coefficient and k2 is integral coefficient.
- The **PWM** signal is generated from the comparator which compares the current error **Δi** with a triangular wave.

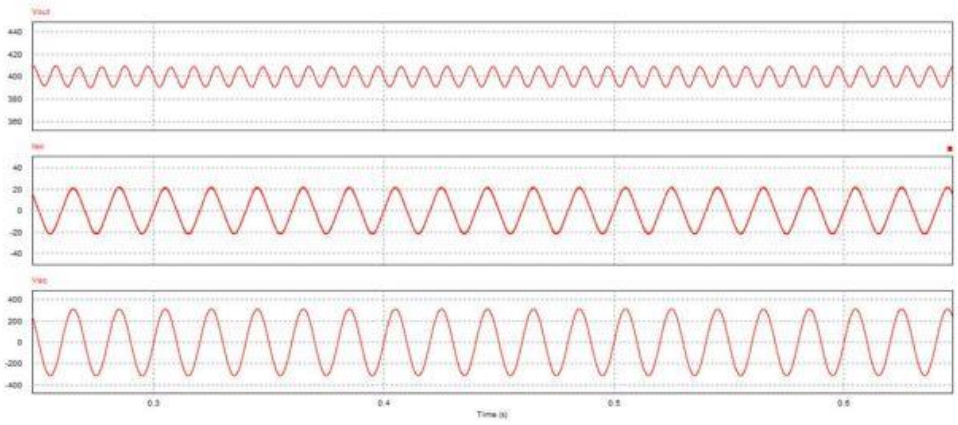

Figure 8: The simulation results – input current and output voltage)

Digital Control and Algorithm

PLL Second Order Generalized Integrator (SOGI)

One of the challenges in Totem Pole PFC design is that the AC line zero crossing point may create shoot through issues. This means that we need to know when the positive cycle transitions to negative cycle. For this the AC line voltage is sensed and sent to the ADC of MCU. A PLL algorithm based on SOGI is adopted. The PLL calculation result can be used to generate the low frequency driver. It is easy to insert the dead time in the low frequency driver pulses. The test result is showed in Figure 9. The Green and Yellow signals are the driver signals of low frequency Si-MOSFET based on the PLL result.

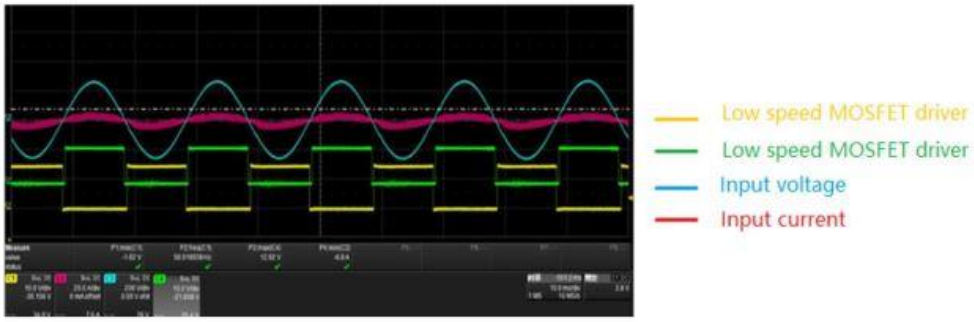

Figure 9: AC Line Voltage Vs. Low Frequency Driver Signal

Soft-start during Zero Crossing

The line current in single-phase PFC topology is distorted at the zero-crossing point of the input AC voltage because of the characteristic of the general proportional integral (PI) current controller. This distortion degrades the line current quality, such as the total harmonic distortion (THD) and the power factor (PFC). There are two main reasons for this distortion.

The first reason is the dynamic response of the PI controller. Given the bandwidth of the PI current controller, its dynamic response is considerably slow. The line current is distorted because the error of the PI controller is considerably large at the zero-crossing point.

The second reason for this distortion is the PFC converter operates in the DCM near the zero-crossing point of the input AC voltage. The line current cannot follow the reference current in this DCM interval, which results in line current distortion. To deal with this issue, the soft-start and dedicated time sequence of the high frequency SiC-MOSFET during zero crossing is adopted in the firmware. With the design, the current has very little zero-crossing distortion, and THD is 2.8% in full load condition.

Figure 10: Soft-start during zero crossing

Current and Voltage Control Loop

In this design, we used a MCU from Spintrol to realize the PFC control and get good results. The algorithm of SOGI PLL, Current loop PI Controller, Voltage loop PI controller and software protection /TZ protection are all realized with the MCU.

A 60kHz interrupt is set in the firmware and PI control loop for current loop is adopted in the design. In PFC applications, it needs a fast-current loop to keep the controlled input current following the input voltage. We choose the bandwidth of the current loop to be 3kHz and phase margin to be 60 degree according the Nyquist stability condition. In the practical application, the cut off frequency of the control loop is set around 0.03~0.25 times of the carrier frequency (switching frequency) to minimize linearization and accuracy limitations in small signal modeling). With dedicated parameters, the final current loop is showed in Figure11. The current is sampled at the average value and it is equivalent to the middle point in each 60kHz switching cycle.

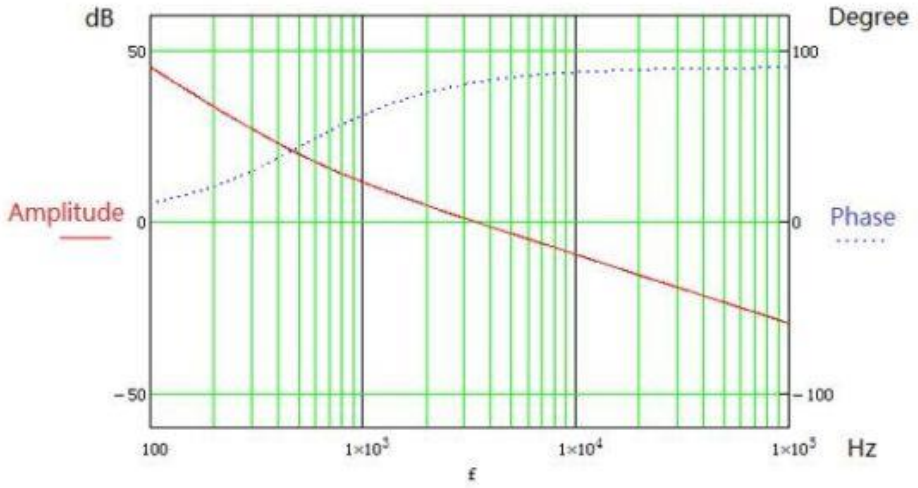

Figure 11: Current loop

A 10kHz interrupt is set in the firmware and the PI control loop is adopted for voltage loop in the design. Because PFC output voltage has two times the line frequency voltage ripple, which results in a third harmonic current, the voltage loop's bandwidth needs be kept low enough to minimize the third harmonic. The bandwidth of voltage loop is set to 10Hz and 60-degree phase margin. The voltage loop must be cut off in low frequency in order to make input current a sine wave. Another 100Hz notch is inserted in the voltage loop to further decrease the third harmonic current.

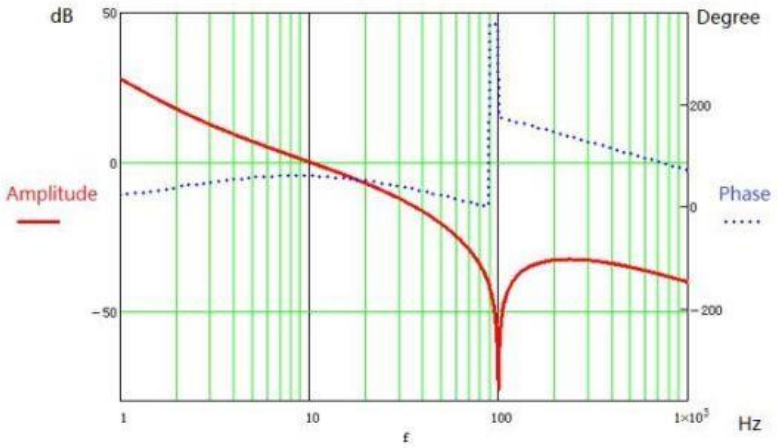

Figure 12: Voltage loop with 100Hz notch

With chosen parameters, the final current loop and voltage loop gain and phase margins are shown in Figure 11 and Figure 12 respectively.

Test Results

Based on the design above, a 3.3KW Totem Pole PFC demo board is built in the lab. The test results and waveforms are showed in the following pictures. 99.1% peak efficiency and 98.5% full load efficiency is achieved in the design, PF 0.998 and THD 2.8% are achieved in full load. From test results, we can see that the selected SiC-MOSFET and high bandwidth current sensor worked well in this application for Totem Pole PFC control and protection with low cost MCU to support 80+Titanium power supplies. Please refer the Figure 13 to Figure 15.

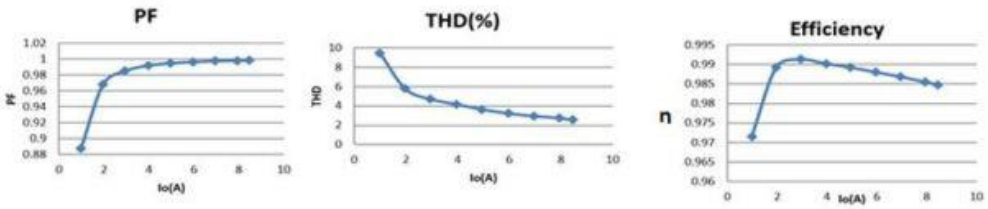

Figure 13: PF, THD and Efficiency values

Figure 14: Input current waveforms @230V for 400W and 1.2kW

Figure 15: Input voltage and current wave forms @180V for 2.4kW and 3.3kW

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6. Reference documents

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2: Calculation of turn-off power losses generated by an ultrafast diode, ST AN5028
3: MCA1101-xx-5 datasheet, ACEINNA